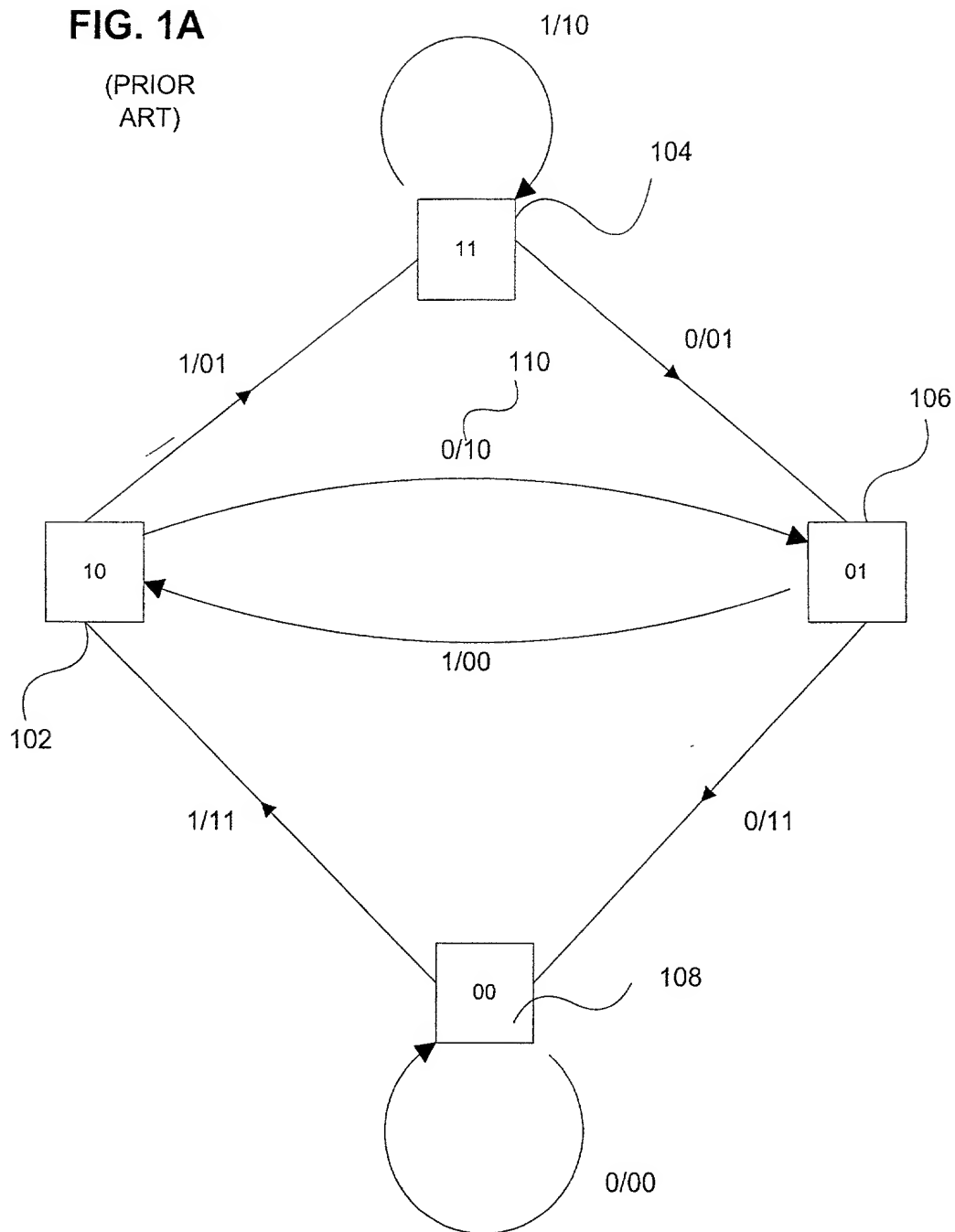


FIG. 1A

(PRIOR
ART)



INPUT BIT	INITIAL STATE	NEXT STATE	OUTPUT CODEWORD
0	00	00	00
1	00	10	11
0	01	00	11
1	01	10	00
0	10	01	10
1	10	11	01
0	11	01	01
1	11	11	10

FIG. 1B (PRIOR ART)

FIG. 2A
(PRIOR ART)

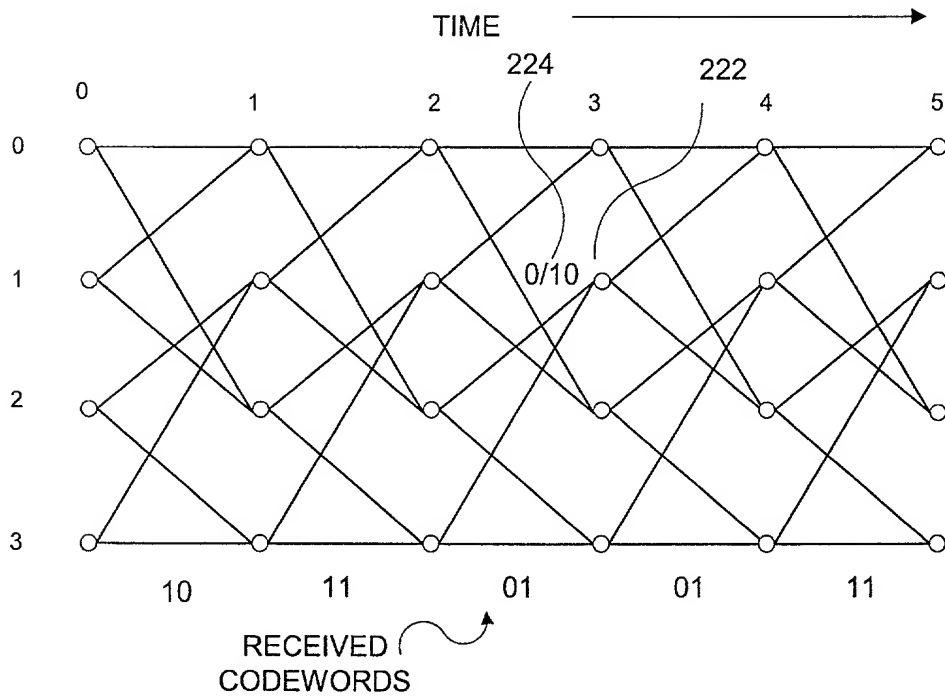
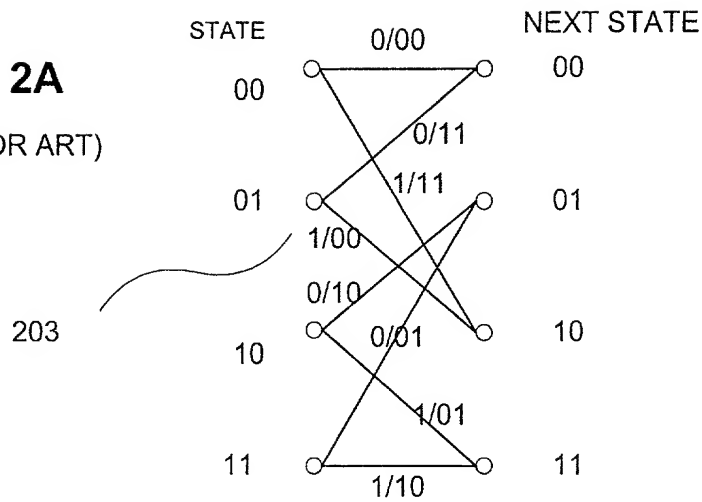


FIG. 2B (PRIOR ART)

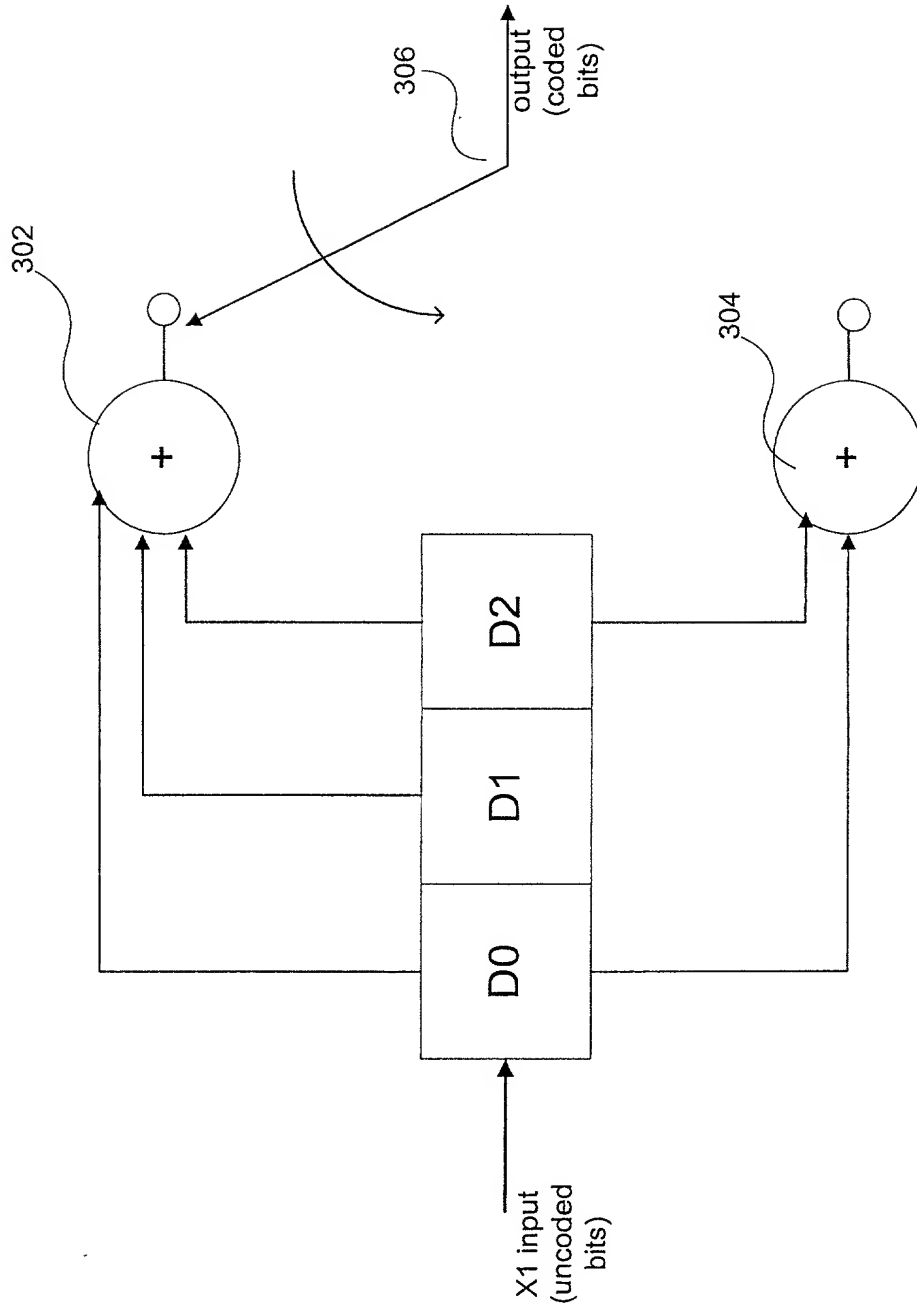


FIG. 3 (Prior Art)

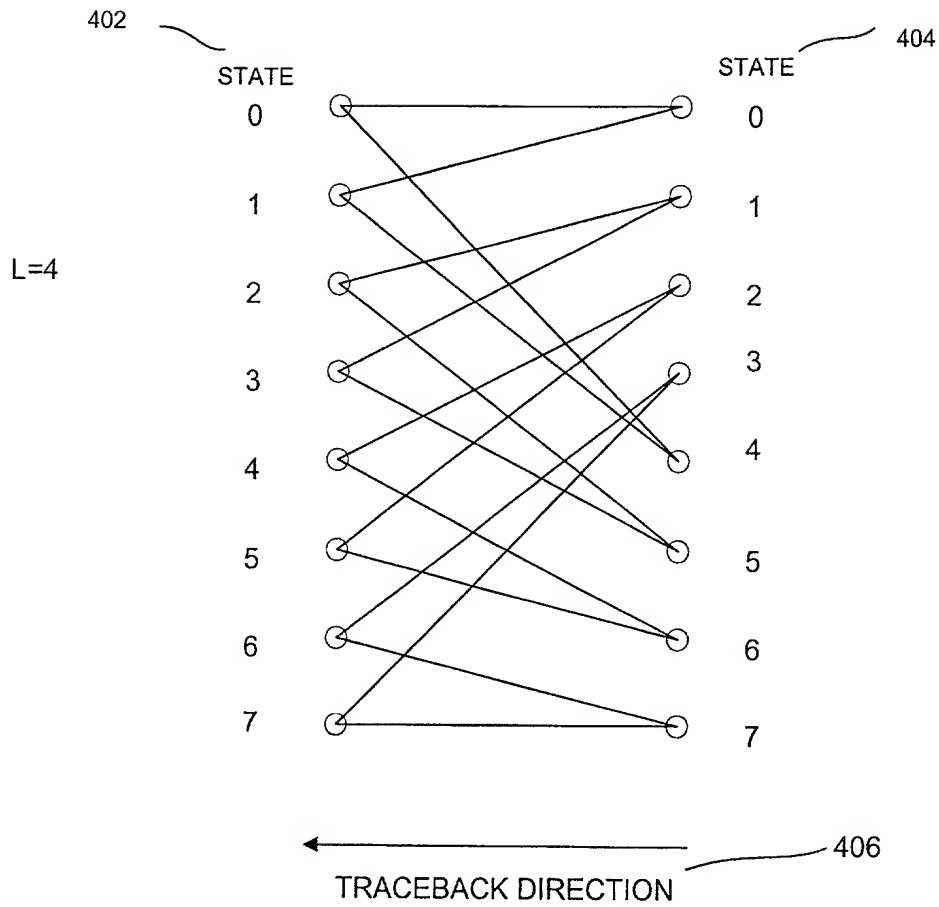


FIG. 4A

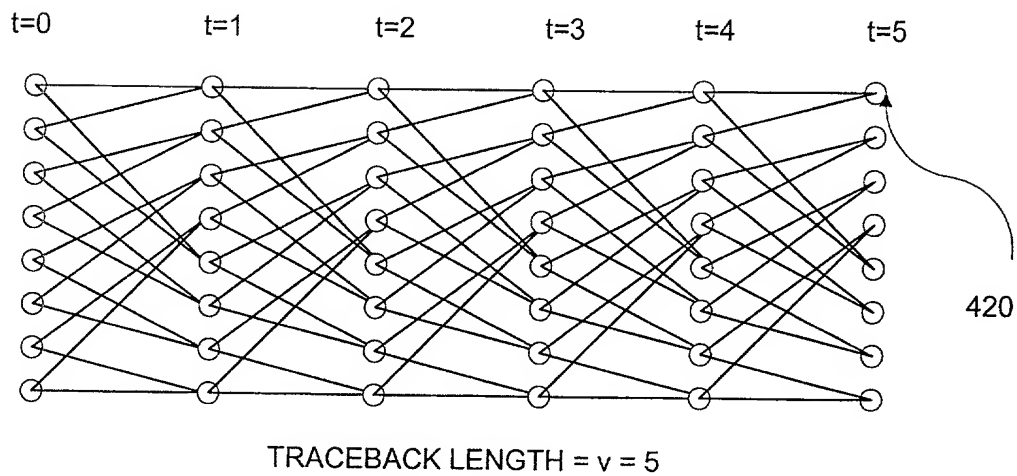


FIG. 4B

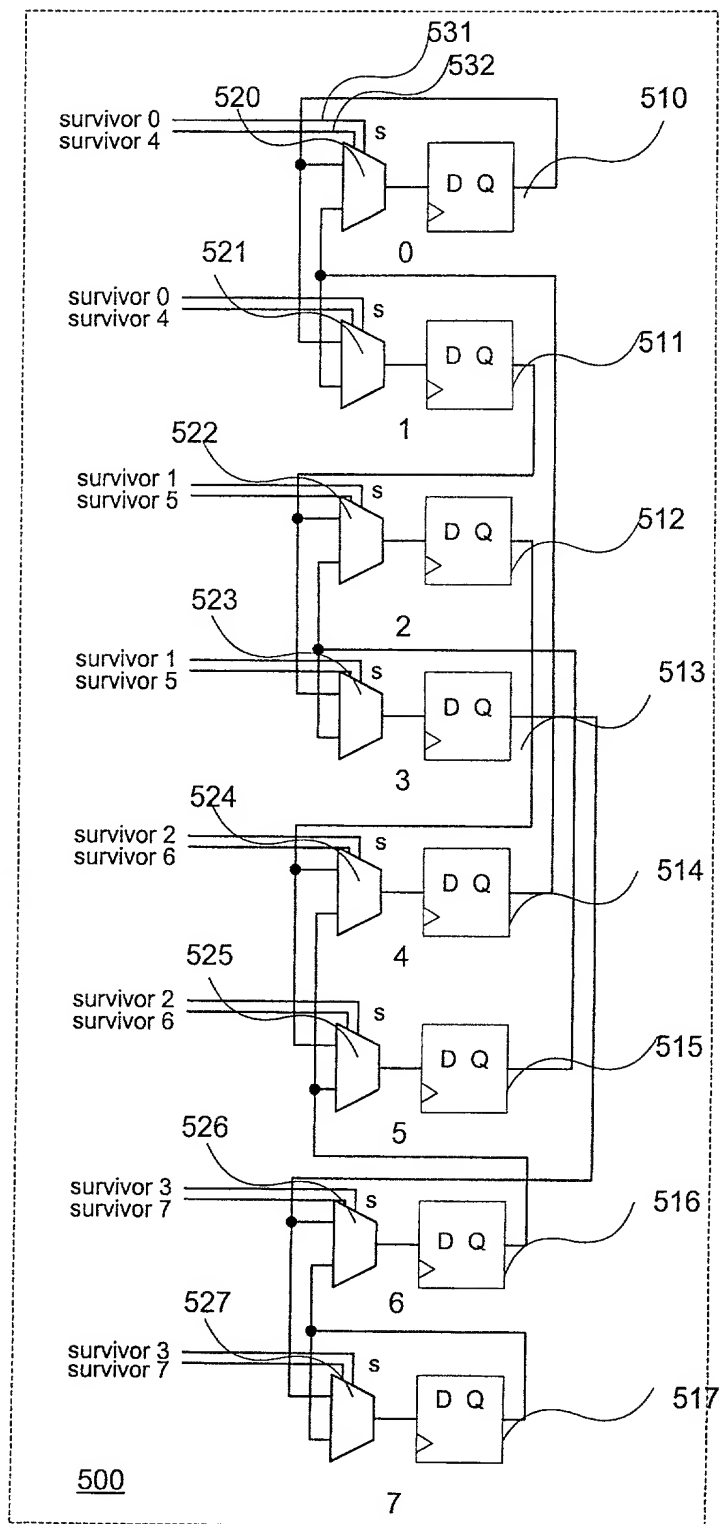
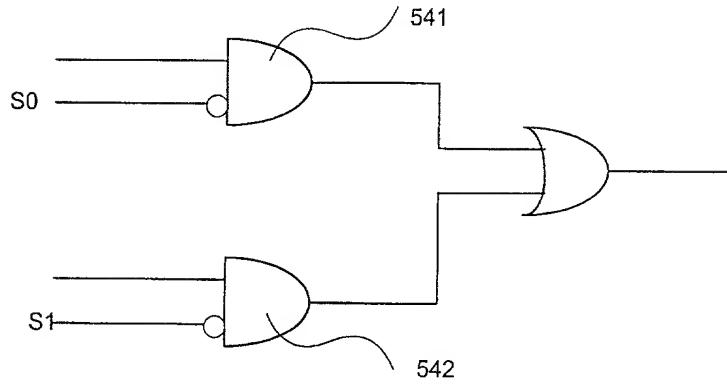


FIG. 5

EVEN MUXES (0, 2, 4, 6)



ODD MUXES (1, 3, 5, 7)

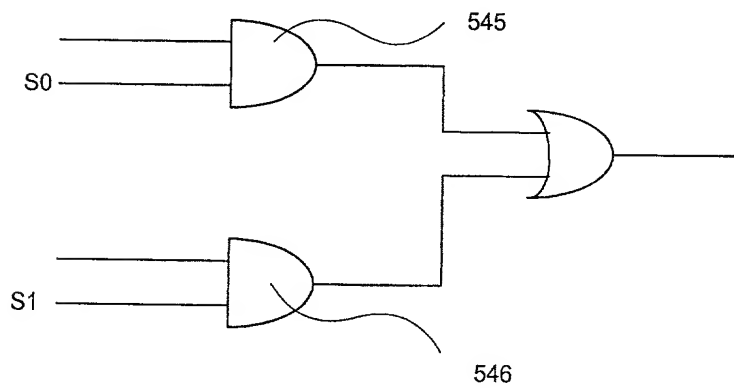


FIG. 5A

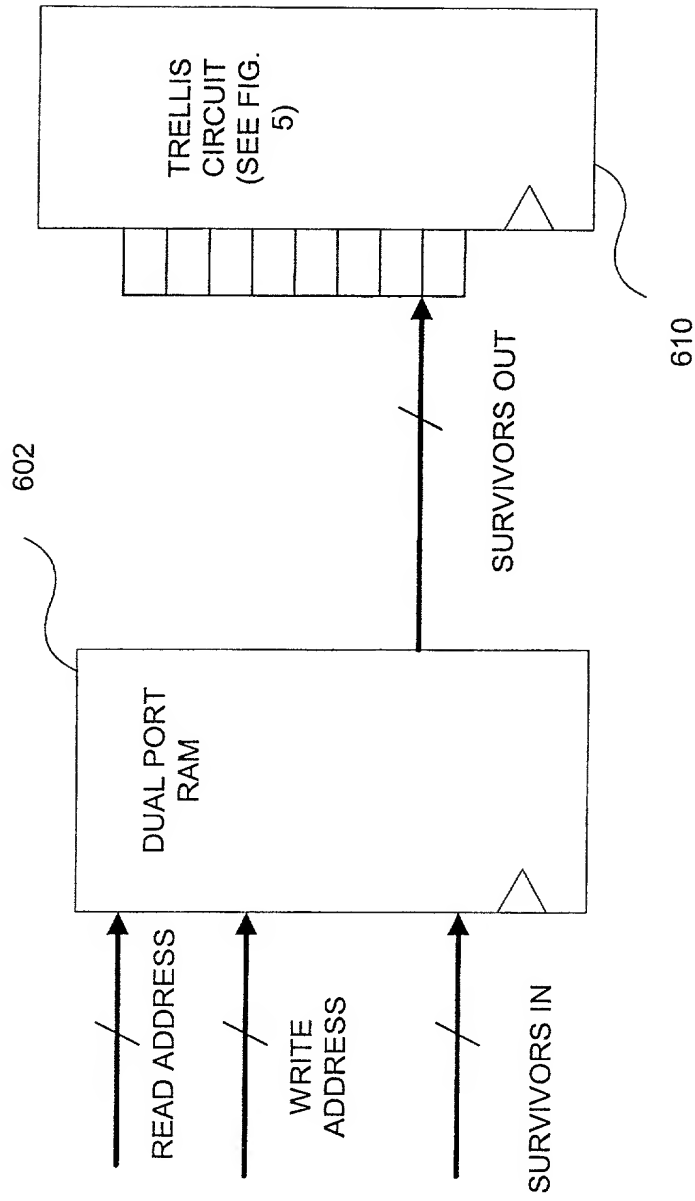


FIG. 6

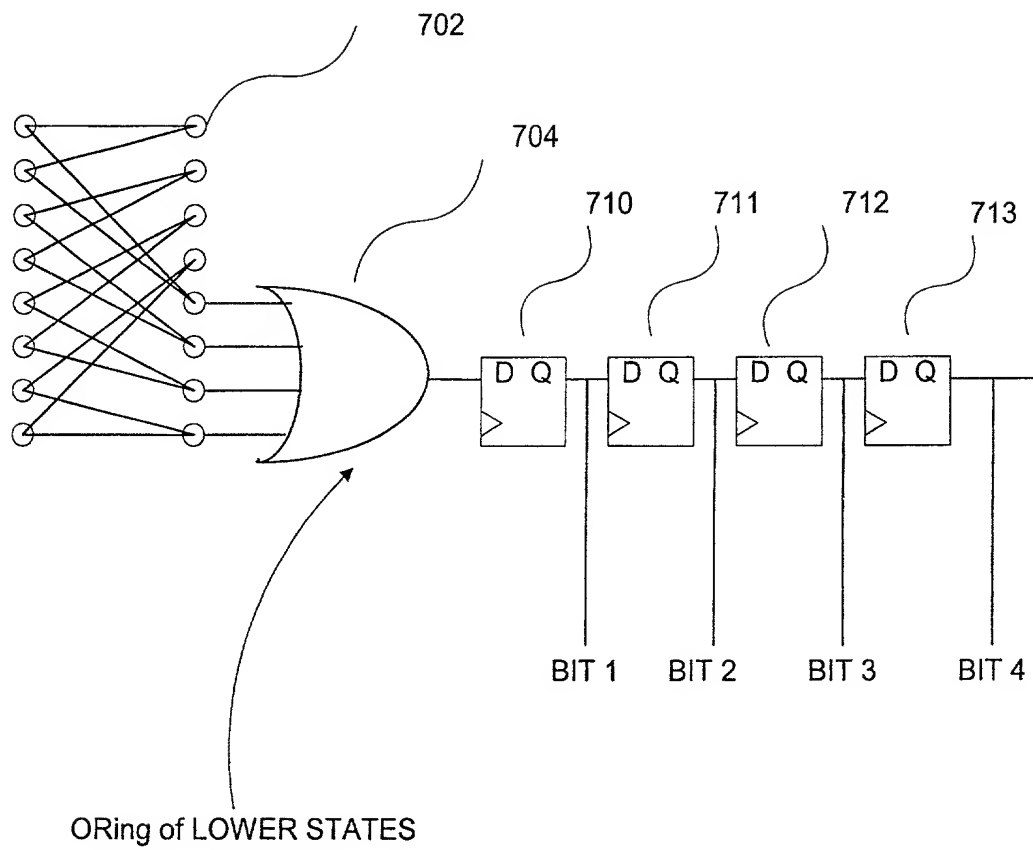
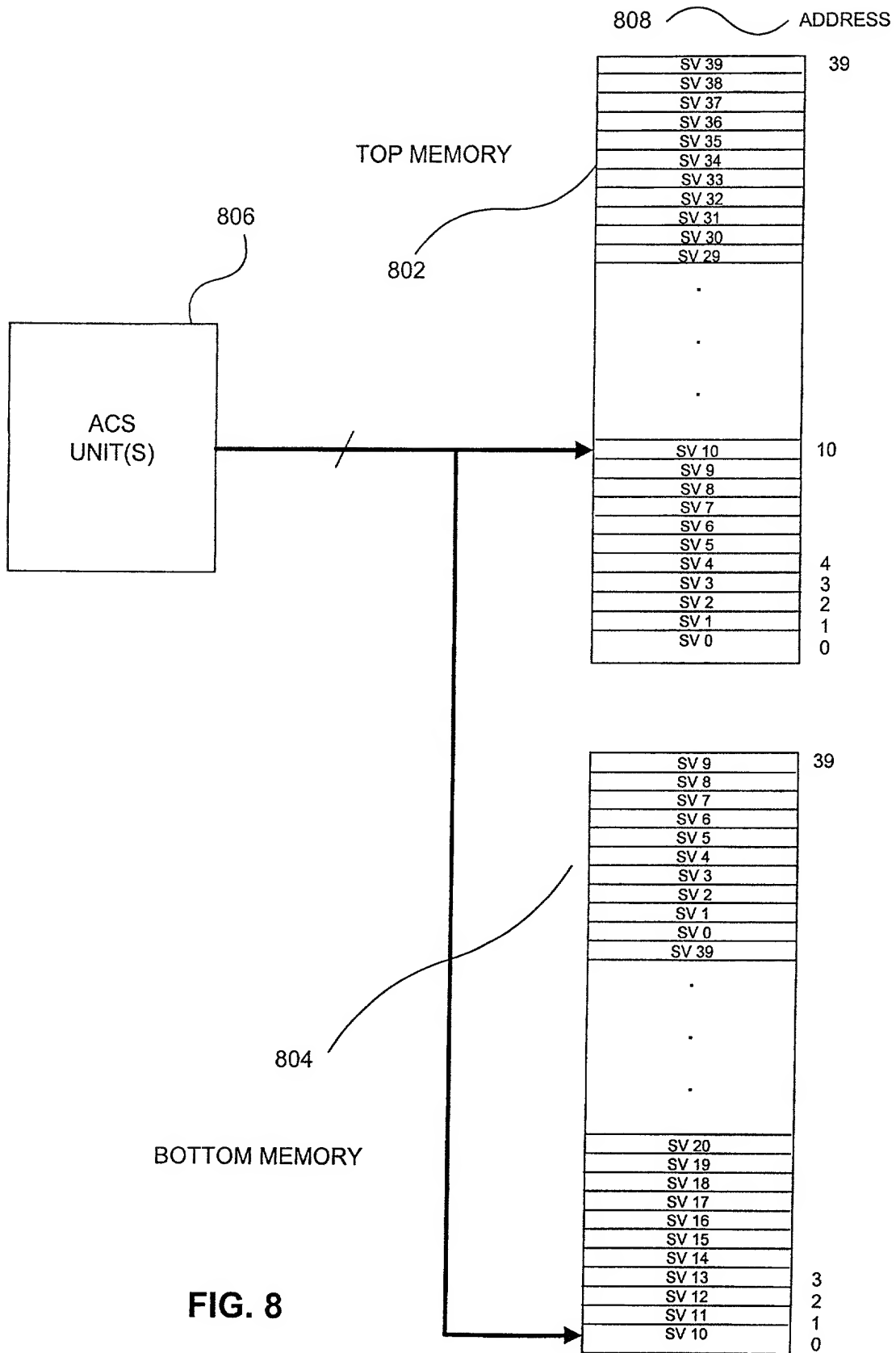


FIG. 7

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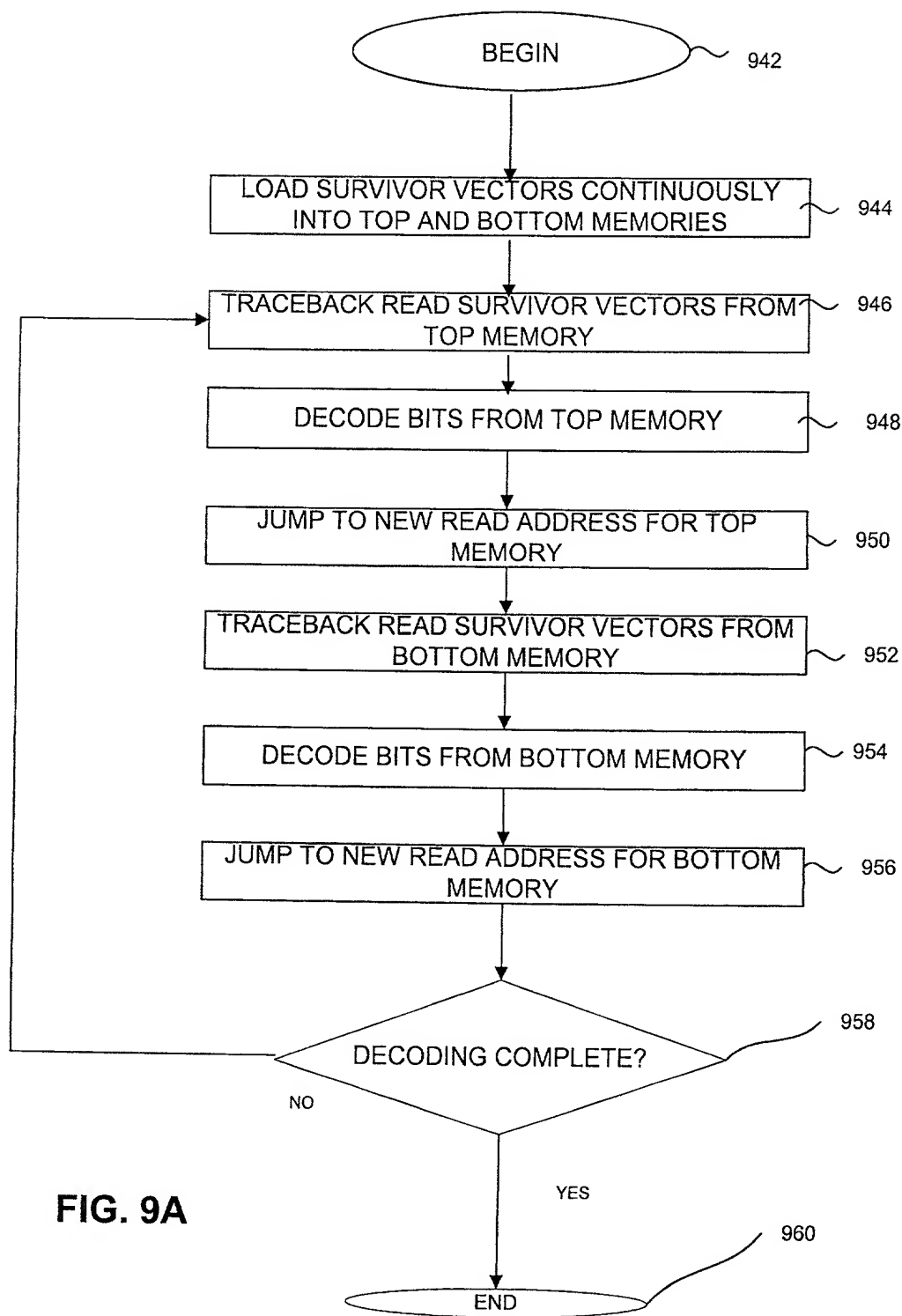


FIG. 9A

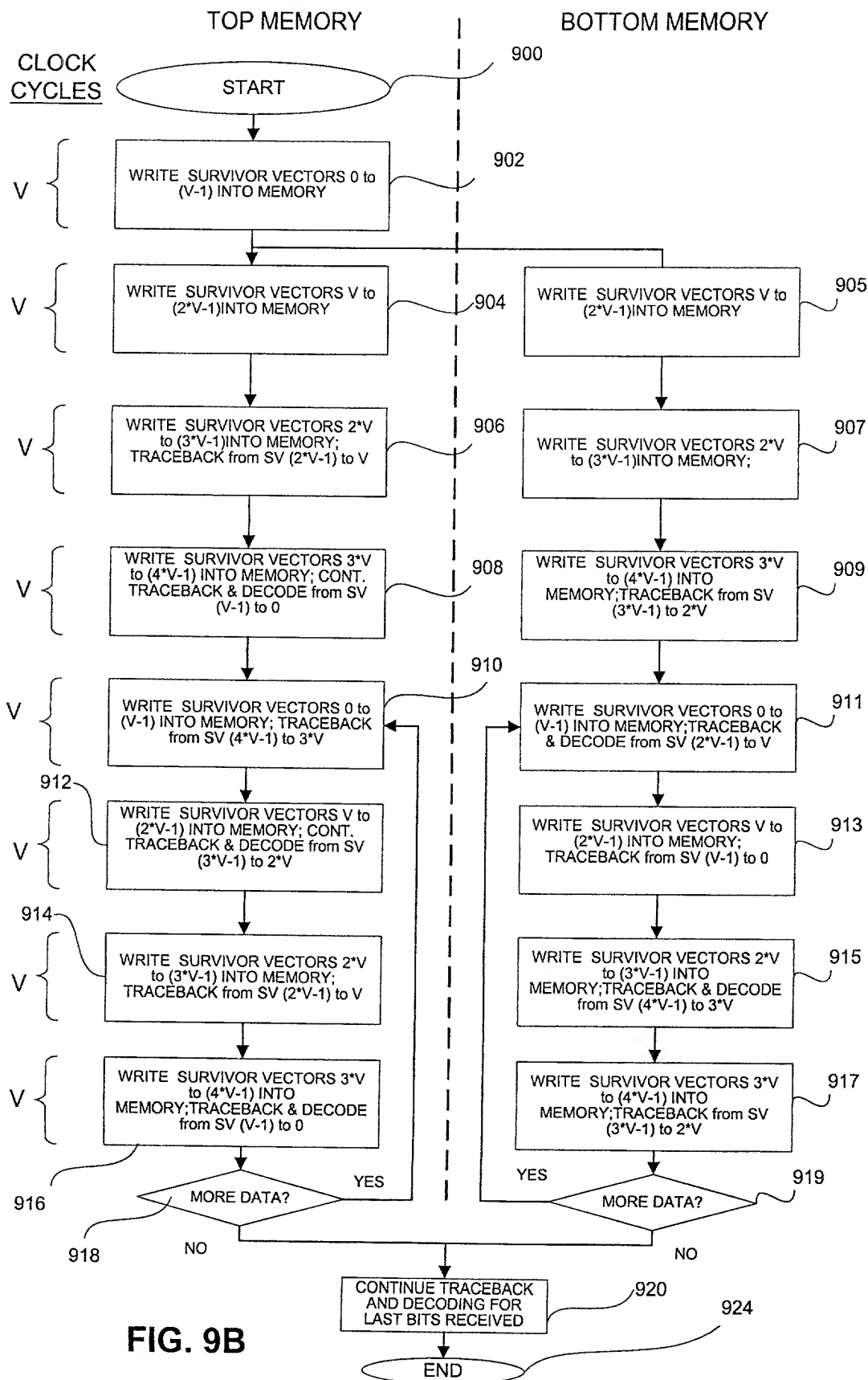


FIG. 9B

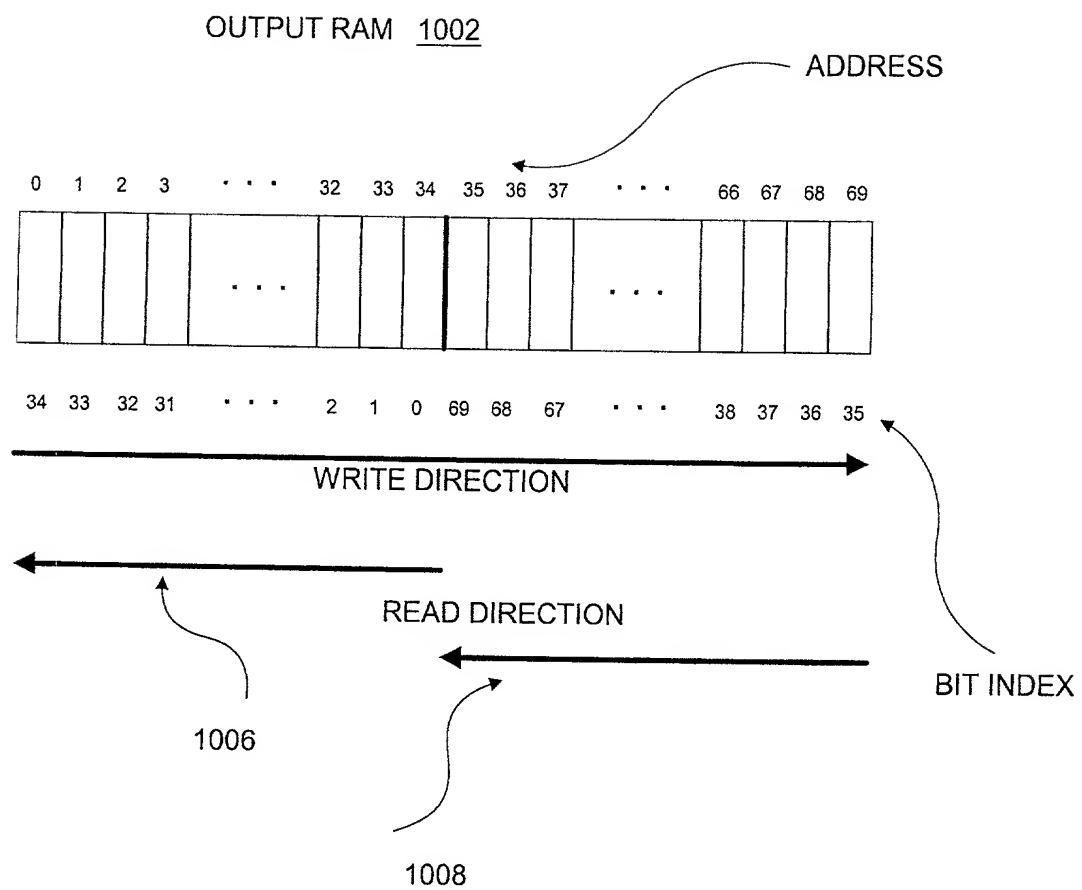


FIG. 10